DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi (JP Publication number 2002-221950) hereinafter Atsushi in view of Kitagawa et al (2002/0063784) hereinafter, Kitagawa.

4. In regards to claim 1, Atsushi teaches a bit rate converter for converting (fig. 1 (10)) an M-bit input (fig. Input into 10) video signal to an N-bit (fig. 1 output of 10) output video signal by retaining grayscale levels (0068-0071), wherein N is smaller than M (0071); and

a pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)), when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10)) corresponds to one of the plurality of N-bit input grayscale levels (0071-0082)

said pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)) delivering one of a plurality of K-bit output grayscale levels to said display device (fig. 1 (13 to 14)).

Atsushi fails to teach a gamma correction memory in which a plurality of N-bit input grayscale levels are mapped to a plurality of K-bit output grayscale levels which are distributed on a non-linear curve corresponding to a non-linear curve on which grayscale levels of a display device are distributed.

However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped (fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020) on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma correction in order to properly show shadow detail in RBG images and to avoid gradation deterioration in gray zones ([0005] of Kitagawa).

5. In regards to claim 3, Atsushi as modified by Kitagawa teaches wherein said K-bit (fig.1 (output to display of Atsushi) output grayscale ([0029] of Kitagawa) levels value, are interpolated grayscale ([0029] of Kitagawa) levels of the N-bit input (fig. 1 (reduced bits from 10) of Atsushi) grayscale levels ([0029] of Kitagawa). Examiner notes the interpolation is part of the non-linear gamma correction as taught by Kitagawa and the N-bits and K-bits are taught by Atsushi, since the gamma correction memory of Kitagawa was substituted.

6. In regards to claim 4, Atsushi teaches wherein K is equal to M (0082) and (fig. 1 (12)).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi and Kitagawa further in view of Lumelsky et al (5,196,924) hereinafter, Lumelsky,

8. In regards to claim 2, Atsushi and Kitagawa discloses the limitations of claim 1,

Atsushi and Kitagawa differ from the claimed invention in that Atsushi does not disclose wherein K is equal to N.

However, Lumelsky discloses K is equal to N. (col. 5, lines 25-25)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to include the use of K is equal to N as taught by Lumelsky in order to further conserve memory.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi in view of Kitagawa further in view of Pether et. al (US 6,801,925) hereinafter, Pether.

10. In regards to claim 5, Atsushi and Kitagawa differ from the claimed invention in that Atsushi and Kitagawa do not disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits.

However, Pether teaches a system and method for wherein said bit rate converter (fig. 5 (100)) comprises means for truncating lower significant bits (fig. 5 of the M-bit video signal (col. 3, lines 49-50), representing the truncated lower significant bits (fig. 5 “LSBs”) by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits. (fig. 5 “error”, 122 and dither col. 4, lines 1-14 of Pether).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to include the use of bit rate converter means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits as taught by Pether in order to provides a means of truncating bits since

Pether uses error feedback and dithering to reduce visual effects as stated in (col. 1, lines 44-50 of Pether).

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi and Kitagawa, in view of Lu et. al (US 7,085,016) hereinafter, Lu.

12. In regards to claim 7, Atsushi and Kitagawa differ from the claimed invention in that Atsushi and Kitagawa do not explicitly disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits.

However, Lu teaches a system and method for wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits (fig. 1 col. 2, lines 57-67 of Lu).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to include the use of dithering as taught by Lu in order to use a process that selects approximate color from a mixture of other colors when transition from pixel data having high bits (M bits) to pixel data having low bits (N bits), since dithering allows for more accurately displaying graphics containing a greater range of colors than the hardware is capable of showing as stated in (col. 1, lines 15-20 of Lu).

13. In regards to claim 8, Atsushi and Kitagawa differ from the claimed invention in that Atsushi and Kitagawa do not explicitly disclose an adder for a binary-1 to higher N bits of the M-bit input video signal; a multiplexer for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal; and a comparator for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value

However, Lu teaches an adder (fig. 5 (24)) for a binary-1 to higher N bits of the M-bit input video signal; a multiplexer (fig. 5 (23)) for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal (col. 3, lines 37-60); and a comparator (fig. 5 (22)) for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value (col. 5-6, lines 37-25).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to include the use of dithering using the particular circuit construction above as taught by Lu in order to use a process that selects approximate color from a mixture of other colors when transition from pixel data having high bits (M bits) to pixel data having low bits (N bits) since dithering allows for more accurately displaying graphics containing a greater range of colors than the hardware is capable of showing as stated in (col. 1, lines 15-20 of Lu).

Allowable Subject Matter

14. Claim 9 is allowed because the prior art does not contain. A bit rate converter comprising an input register for receiving an M-bit input video signal; a first adder for adding a binary-1 to a least significant bit position of a higher N bits of the M-bit input video signal; a first multiplexer for selecting an output of said first adder or said higher N bits in response to a first control signal; a first frame memory for storing an output of said first multiplexer; a second adder for adding a binary-1 to an output of the first frame memory; a second multiplexer for selecting an output of said second adder or an output of said first frame memory in response to a second control signal; a second frame memory for storing an output of said second multiplexer; a third adder for adding a binary-1 to an output of the second frame memory; a third multiplexer for selecting an output of said third adder or an output of said second frame memory in response to a third control signal; a third frame memory for storing an output of said third multiplexer; and controller producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on truncated lower significant bits of the M-bit video signal.

15. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not contain a bit rate converter comprises: a first adder for a binary-1 to the least significant bit position of higher N bits

of the M-bit input video signal; a first multiplexer for selecting an output of said first adder or said higher N bits in response to a first control signal; a first frame memory for storing an output of said first multiplexer; a second adder for, a binary-1 to an output of the first frame memory; a second multiplexer for selecting an output of said second adder or an output of said first frame memory in response to a second control signal; a second frame memory for storing an output of said second multiplexer; a third adder for summing a binary-1 to an output of the second frame memory; a third multiplexer for selecting an output of said third adder or an output of said second frame memory in response to a third control signal; a third frame memory for storing an output of said third multiplexer; and control means for producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on the truncated lower significant bits.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Adachi (6,903,732) –discusses using gamma correction with subtractive color process and a dither method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/GDS/
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